**IN THE CLAIMS:**

Please amend claims 10 and 20 as indicated in the following.

**Claims Listing:**

1. – 9. (Canceled)

10. (Currently Amended) ~~The SRAM device as set forth in Claim 1 wherein~~ A static random access memory (SRAM) device capable of storing a program that is accessible when said SRAM device is powered up, said SRAM device comprising a plurality of storage cells, each of said storage cells comprising:

a data latch having a first input/output (I/O) line and a second I/O line, said data latch comprising:

a first inverter having an input coupled to said first I/O line and an output coupled to said second I/O line; and

a second inverter having an input coupled to said second I/O line and an output coupled to said first I/O line; and

a biasing circuit capable of forcing at least one of said first and second I/O lines to a known logic state when power is applied to said SRAM device, wherein said known logic state comprises a portion of said program, said biasing circuit ~~comprises~~ comprising a grounding circuit selectively connected by a programmable connect to one of said first inverter output and said second inverter output, wherein said grounding circuit is temporarily enabled after power is applied to said SRAM device, thereby grounding one of said first inverter output and said second inverter output and forcing said second I/O line to said known logic state.

11. – 19. (Canceled)

20. (Currently Amended) ~~The data processor as set forth in Claim 11 wherein~~ A data processor comprising a central processing unit (CPU) capable of executing a boot-up program when power is applied to said CPU, said CPU comprising:

a static random access memory (SRAM) device capable of storing said boot-up program, said SRAM device comprising a plurality of storage cells capable of storing ~~bits of~~ said boot-up program, each of said storage cells comprising:

a data latch having an input and an output, said data latch comprising:

a first inverter having an input coupled to said first I/O line and an output coupled to said second I/O line; and

a second inverter having an input coupled to said second I/O line and an output coupled to said first I/O line; and

a biasing circuit capable of forcing at least one of said first and second I/O lines to a known logic state when power is applied to said SRAM device, wherein said known logic state comprises a portion of said boot-up program, said biasing circuit ~~comprises~~ comprising a grounding circuit selectively connected by a programmable connect to one of said first inverter output and said second inverter output, wherein said grounding circuit is temporarily enabled after power is applied to said SRAM device, thereby grounding one of said first inverter output and said second inverter output and forcing said second I/O line to said known logic state.

21. (Canceled)

22. (Canceled)